REMARKS/ARGUMENTS

Claims 1-30 are pending in the present application.

This Amendment is in response to the Final Office Action mailed July 12, 2005. In the Final Office Action, the Examiner rejected claims 1-30 under 35 U.S.C. §103(a). Reconsideration in light of the remarks made herein is respectfully requested.

Responses to Examiner's Arguments

In the Final Office Action, the Examiner contended that a bus does not have to be external to a device. To support for his contention, the Examiner provided a definition from Microsoft Press Computer Dictionary, Second Edition, and stated that "[n]either by this definition, nor by any other definition given in the disclosure, is a bus required to be external to a device." (Final Office Action, Page 2, Paragraph No. 3). However, the very definition provided by the Examiner indicates that the bus has to be external to a device in order to be shared by other parts of the system:

> "...A bus is essentially a shared highway that connects different parts of the system – including the microprocessor, disk-drive controller, memory, and input/output ports – and enables them to transfer information."
> (Microsoft Press Computer Dictionary – Second Edition)

Since a bus is shared by these devices, it has to be external to a device. An internal bus cannot be shared by other devices. The specification also clearly shows the master bus 115_1 to 115_N as external to all devices.

Furthermore, the host interfaces in Hubbins device cannot operate as a bus master. A master bus is a bus that multiple masters are connected. Since each master is able to control the bus by virtue of issuing address and data, the master bus is inherently bi-directional as shown by bi-directional arrows in Figures 1 and 3 in the Specification. In contrast, Hubbins merely discloses a host interface that receives address information and acts like a slave device to the processor by virtue of occupying 8 register locations in the address space of the processor (Hubbins, col. 3, lines 39-41; Figure 2, host interfaces 2 and 3). As such the host interfaces 2 and 3 are not master buses.

The Examiner further contended that the connection between the MUX and the memory (interpreted as a slave to the processors) is a slave bus (Final Office Action, Page 2, Paragraph No. 3, bottom three lines). Applicants respectfully disagree. As defined above in the Microsoft Press Computer Dictionary, a bus is shared by different parts of a system. Here, as clearly shown in Figure 2 of Hubbins, the connections between the multiplexers MUXes 18 and 21 are directly to the address lines and the data lines of the RAM device 1. No sharing is possible. The address and data lines between the MUXes 18 and 21 to the RAM 1 are not made available to the external world. Furthermore, since the RAM, the arbitration latch, and the host interfaces are all housed in a single device, it is impossible for another device to share the address and data lines between the MUXes 18 and 21 and the RAM. Accordingly, the connection between the MUX and the memory cannot be a slave bus.

Furthermore, a slave bus is defined in the specification as a bus capable of being connected by a plurality of slave devices (See specification, paragraph [0016]). Here, the RAM is the only device connected to the MUXes. Therefore, Hubbins does not disclose, suggest, or render obvious a multiplexer coupled to a slave bus.

The Examiner further contended that Burgess discloses an address decoder that generates a device select signal (Final Office Action, Page 3, Paragraph No. 4). Applicants respectfully disagree. As argued in the previous response, Burgess merely discloses an address decoder to pair a device with an address selected line, NOT to decode the slave address and NOT to generate the device select signal. (Emphasis added.) As is known by one of ordinary skill in the art, "pairing" is not the same as "decoding" an address or "generating" a signal.

The Examiner further contended that the selector of Opoczynski reads on the limitations of the claims because a multiplexer is a hardware circuit for selecting a single output from multiple inputs which is shown in both Figure 3 of Opoczynski and Figure 3 of the instant application (Final Office Action, Pages 3 and 4, Paragraph No. 5). Applicants respectfully disagree. Opoczynski merely discloses a selector which controls which of the line drivers/receivers circuits receive the serial port I/O stream. In essence, it connects the serial port I/O stream from the serial port 44 to one of the drivers/receivers 48A and 48B. Therefore, it does not select a single output from multiple inputs and cannot function as a multiplexer. Furthermore, even if it may function as a multiplexer, it does not provide bus response

information from device response information. As discussed above, it merely connects the serial port I/O stream to one of the drivers/receivers. A serial port is not a bus.

The Examiner further contends that Leedom teaches a common memory interface to allow multiple devices access to common memory (Final Office Action, Pages 4 and 5, Paragraph No. 6). However, Applicants do not claim a common memory interface by itself. Claims 6, 16, and 26 recite the plurality of slave buses being coupled to a common memory via a common memory interface. The common memory is accessible to all master processors or slave devices (See, for example, Specification, paragraph [0017]). Since Hubbins, Burgess, or Opoczynski does not, individually or in combination, disclose or suggest a plurality of slave buses and a common memory, and Leedom does not disclose a common memory used as a slave device, the combination of Hubbins, Burgess, Opoczynski, and Leedom is improper.

Rejection Under 35 U.S.C. § 103

In the Final Office Action, the Examiner rejected claims 1-30 under 35 U.S.C. §103(a). Applicants respectfully traverse the rejection and contend that the Examiner has not met the burden of establishing a prima facie case of obviousness. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *MPEP §2143, p. 2100-129 (8th Ed., Rev. 2, May 2004).* Applicants respectfully contend that there is no suggestion or motivation to combine their teachings, and thus no *prima facie* case of obviousness has been established.

1) Claims 1-2, 11-12, and 21-22:

Claims 1-2, 11-12, and 21-22 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,698,753 issued to Hubbins et al. ("Hubbins").

Hubbins discloses a multiprocessor interface device. The device has ports A and B connected respectively to the bus systems of processors A and B and the ports are connected to a multiplexer to a common memory (Hubbins, col. 3, lines 29-31). The device has mode pins to

define 4 modes. In the master and slave mode, the devices may be employed in parallel to accommodate wider word length (Hubbins, col. 10, lines 5-23).

The Examiner states that Hubbins discloses a multiplexer coupled to the first and second processors and to a slave, in this case the memory (Final Office Action, page 6, lines 1-2, Paragraph No. 9). Applicants respectfully disagree.

First, as clearly shown in Figure 1 in Hubbins, the multiplexer is merely connected to ports A and B and a 256x8 RAM. Ports A and B are contained inside the device (Hubbins, col. 3, lines 60-65; Figure 2, elements 2, 3, and 1). Since the ports are inside the device, they cannot be master buses. A master bus should be outside of a device to provide interface access to a plurality of other processors.

Furthermore, the host interfaces at ports A and B in Hubbins device cannot operate as a bus master. A master bus is a bus that multiple masters are connected. Since each master is able to control the bus by virtue of issuing address and data, the master bus is inherently bi-directional. Here, Hubbins merely discloses a host interface that receives address information and acts like a slave device to the processor by virtue of occupying 8 register locations in the address space of the processor (Hubbins, col. 3, lines 39-41; Figure 2, host interfaces 2 and 3). Therefore, the host interfaces 2 and 3 are not master buses.

Second, there is no slave bus. The memory is connected directly to the multiplexer. As defined above in the Microsoft Press Computer Dictionary, a bus is shared by different parts of a system. Here, as clearly shown in Figure 2 of Hubbins, the connections between the multiplexers MUXes 18 and 21 are directly to the address lines and the data lines of the RAM device 1. No sharing is possible. The address and data lines between the MUXes 18 and 21 to the RAM 1 are not made available to the external world. Furthermore, since the RAM, the arbitration latch, and the host interfaces are all housed in a single device, it is impossible for another device to share the address and data lines between the MUXes 18 and 21 and the RAM. Accordingly, the connection between the MUX and the memory cannot be a slave bus.

Furthermore, a slave bus is defined in the specification as a bus capable of being connected by a plurality of slave devices (See specification, paragraph [0016]). Here, the RAM is the only device connected to the MUXes. Therefore, Hubbins does not disclose, suggest, or render obvious a multiplexer coupled to a slave bus.

The Examiner further states that while Hubbins does not explicitly teach that there is a plurality of slave buses, he does teach that several devices can be used in parallel (Final Office Action, page 6, Paragraph 9). Applicants respectfully disagree. Using several devices in parallel does not mean that a plurality of slave buses exists. Arranging these devices in parallel merely expands the width of the word length, e.g., from D0 – D7 to D0 – D7, D8 – D15, and D16 – D23 (Hubbins, Figure 9).

In summary, Hubbins effectively teaches away from the invention because all the interface circuits are located internally to a device. The host interfaces to ports A and B are not master buses. There are no a plurality of slave buses. Even if there is a slave bus, the slave bus is not connected to a plurality of devices.

2) Claims 3, 13, and 23:

Claims 3, 13, and 23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hubbins as applied to claims 1-2 above, and further in view of U.S. Patent No. 5,590,369 issued to Burgess et al. ("Burgess").

Hubbins is discussed above.

Burgess discloses a bus supporting a plurality of data transfer sizes and protocols. A peripheral bus (Pbus) is used for transferring data between a processor and various peripheral devices (also denoted slaves) (Burgess, col. 4, lines 47-51). A Pbus master controls the operation of the Pbus (Burgess, col. 4, lines 52-54). The address bus connects the Pbus master with a synchronous/ asynchronous address decoder (Burgess, col. 6, lines 19-21). This decoder pairs each slave device with a corresponding address selected line connected to the slave(s) involved in the data transfer (Burgess, col. 6, lines 25-28).

Hubbins and Burgess, taken alone or in combination, do not disclose, suggest, or render obvious an address decoder coupled to the bus arbiter and the first mutiplexer to decode the slave address. As discussed above, Hubbins does not disclose a first multiplexer coupled to first and second master buses and slave address. Burgess merely discloses an address decoder to pair each slave device with a corresponding address selected line, not to decode a slave address in a plurality of slave buses.

Furthermore, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). MPEP 2143.01. Here, Hubbins discloses a single memory inside a device. Modifying the device to include the address decoder to access multiple devices as provided by Burgess would render Hubbins device unsatisfactory because its intended purpose is to allow accessing to a single memory, not a plurality of memories (Hubbins, col. 3, lines 29-32).

3) Claims 4-5 and 7-10, 14-15 and 17-20, and 24-25 and 27-30:

Claims 4-5 and 7-10, 14-15 and 17-20, and 24-25 and 27-30 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hubbins and Burgess as applied to claim 3 above, and further in view of U.S. Patent No. 5,453,737 issued to Opoczynski ("Opoczynski").

Hubbins and Burgess are discussed above.

Opoczynski discloses a control and communication apparatus. A master controller communicates with a plurality of slave subsystems (Opoczynski, col. 2, lines 25-27). A serial port is connected through a selector, which receives a select line from the controller processor and controls which of the line drivers/receivers circuits receive the serial port I/O stream (Opoczynski, col. 3, lines 65-67; col. 4, line 1).

Hubbins, Burgess, and Opoczynski, taken alone or in any combination, do not disclose, suggest, or render obvious (1) a second multiplexer coupled to the first slave bus to provide bus response information from device response information using the device select signal; and (2) a de-multiplexer coupled to the second multiplexer and the first and second master buses to transfer the bus response information to one of the first and second processors using the arbitration select signal. As discussed above, Hubbins does not disclose a first multiplexer coupled to first and second master buses and slave address. Burgess does not disclose an address decoder to decode slave address. Opoczynski merely discloses a selector to control which of the line drivers/receivers receives the serial port I/O stream. The serial port I/O stream is not the same as the bus response information from device response information. Furthermore, the selector is not connected to a first slave bus that is also connected to another multiplexer.

The Examiner states that Opoczynski teaches a selector (multiplexer) that selects data from multiple data buses for I/O, and the multiplexer 21 of Figure 2 of Hubbins, while labeled a multiplexer, actually performs as de-multiplexer (Final Office Action, Page 7, lines 1-4, Paragraph No. 12). Applicants respectfully disagree for the following reasons.

As discussed above, Opoczynski merely discloses a selector which controls which of the line drivers/receivers circuits receive the serial port I/O stream. In essence, it connects the serial port I/O stream from the serial port 44 to one of the drivers/receivers 48A and 48B. Therefore, it does not select a single output from multiple inputs and cannot function as a multiplexer. Furthermore, even if it may function as a multiplexer, it does not provide bus response information from device response information. It merely connects the serial port I/O stream to one of the drivers/receivers. The serial port I/O stream is not the bus response information. A serial port is not a bus.

Regarding the multiplexer 21 in Hubbins, even if this device function as a de-multiplexer, it merely transfers the data output of the RAM (Hubbins, col. 4, lines 36-38), not the bus response information from the device response information. The bus response information may include address, data, device ready signal (See, for example, Specification, paragraph [0032], Figure 3).

4) Claims 6, 16, and 26:

Claims 6, 16, and 26 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hubbins, Burgess and Opoczynski as applied to claim 4-5 and 7-10 above, and further in view of U.S. Patent No. 5,717,8957 issued to Leedom et al. ("Leedom").

Leedom discloses an associative scalar data cache with write-through capabilities for a vector processor. A scalar/vector supercomputer includes a scalar/vector processor connected through a common memory interface to one or more sections of common memories (Leedom, col. 5, lines 19-23).

Hubbins, Burgess, Opoczynski, and Leedom, taken alone or in any combination, do not disclose, suggest, or render obvious the plurality of slave buses being coupled to a common memory via a common memory interface. As discussed above, Hubbins, Burgess, and Opoczynski, individually or collectively, do not disclose first and second master buses, a

plurality of slave buses, a multiplexer, an address decoder, a second multiplexer, and a de-multiplexer. Leedom merely discloses a common memory interface to a scalar/ vector processor. A scalar/ vector processor is not a slave device connected to a slave bus. The common memory interface in Leedom is connected directly to the V registers, the B and T registers, the address selector, and the instruction buffers (Leedom, Figure 1), not to a plurality of slave buses. Since none of Hubbins, Burgess, and Opoczynski discloses or suggests master buses and a plurality of slave buses, and Leedom does not disclose or suggest a common memory interface coupled to a plurality of slave buses, the combination of these prior art references is improper.

In summary, the Examiner has not met the burden of establishing a prima facie case of obviousness in rejecting claims 1-30 under 35 U.S.C. §103(a). "When determining the patentability of a claimed invention which combined two known elements, 'the question is whether there is something in the prior art as a whole suggest the desirability, and thus the obviousness, of making the combination.'" In re Beattie, Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 1462, 221 USPQ (BNA) 481, 488 (Fed. Cir. 1984). To defeat patentability based on obviousness, the suggestion to make the new product having the claimed characteristics must come from the prior art, not from the hindsight knowledge of the invention. Interconnect Planning Corp. v. Feil, 744 F.2d 1132, 1143, 227 USPQ (BNA) 543, 551 (Fed. Cir. 1985). To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the Examiner to show a motivation to combine the references that create the case of obviousness. In other words, the Examiner must show reasons that a skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the prior elements from the cited prior references for combination in the manner claimed. In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1996), 47 USPQ 2d (BNA) 1453. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or implicitly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973. (Bd.Pat.App.&Inter. 1985). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680,

16 USPQ2d 1430 (Fed. Cir. 1990). Furthermore, although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so." In re Mills 916 F.2d at 682, 16 USPQ2d at 1432; In re Fitch, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992). When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to: (A) The claimed invention must be considered as a whole; (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (D) Reasonable expectation of success is the standard with which obviousness is determined. Hodosh v. Block Drug Col, Inc., 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986). Here, none of the cited prior art references discloses or suggests the desirability of the combination. Furthermore, the Examiner has failed to present a convincing line of reasoning as to why the claimed invention is obvious in light of the teachings of Hubbins, Burgess, Opoczynski, and Leedom, either individually or in any combination.

Therefore, Applicants believe that independent claims 1, 11, 21 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejections under 35 U.S.C. §103(a) be withdrawn.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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